Listing of Claims:

Claim 1 (currently amended): An interposer for compliantly connecting a chip die directly to a circuit card comprising a layer of elastic dielectric material having an array of ~~metal~~ copper plated vias filled with solder extending from one surface of said dielectric material to the other with each of said ~~metal~~ copper plated vias terminating in a ~~metal~~ copper pad at said one and said other surface and with each of said ~~metal~~ copper plated vias similarly sloped with respect to said one and said other surface so as to allow said interposer to flex both vertically and horizontally, said layer of elastic dielectric material further having a uniform array of holes extending therethrough and arranged so that individual ones of said holes of said array of holes are positioned to be substantially surrounded by individual ones of said array of copper plated vias so as to further facilitate uniform compliance of said interposer.

Claim 2 (canceled)

Claim 3 (currently amended) The interposer as set forth in Claim ~~2~~ 1 wherein said elastic dielectric material ~~has~~ having an array of holes extending therethrough positioned ~~between~~ to be surrounded by individual ones of said array of copper plated vias are arranged with a slope substantially the same as the slope of said copper plated vias.

Claim 4 (original) The interposer as set forth in Claim 3 wherein said elastic dielectric material is 10 to 15 mils thick and has an elastic modulus in the range of 50,000 to 400,000 psi.

5. (currently amended) An electronic package comprising:

a semiconductor chip die having an array of conductive pads on one surface thereof;

a flexible layer of dielectric material having an array of metal plated vias extending therethrough in similarly sloped relationship to opposing surfaces thereof with said metal plated vias of said array of metal plated vias formed by two segments each of which is sloped with respect to an opposing surface of said flexible layer of dielectric material to meet internal to said surfaces to form a V-shaped metal plated via so as to thereby allow said layer of dielectric material to flex both vertically and horizontally and with each of said metal plated vias terminating in a metal pad on each of said opposing surfaces to form an array of pads thereon with respective ones of said metal pads on one of said opposing surfaces electrically connected to respective ones of said array of conductive pads on said chip die, said flexible layer of dielectric material having a uniform array of holes extending therethrough arranged so that individual ones of said holes of said array of holes are positioned to be substantially surrounded by individual ones of said array of copper plated vias; and

a circuit card having an array of conductive pads corresponding to said array of metal pads on the other of said opposing surfaces of said flexible layer of dielectric material with respective ones of said array of conductive pads on said circuit card

electrically connected to respective ones of said array of metal pads on the said other of said opposing surfaces of said layer of dielectric material.

Claim 6. (currently amended) The electronic package of Claim 5 wherein said array of metal plated vias each terminating in a metal pad on each of said opposing surfaces is an array of copper plated vias each terminating in a copper pad on each of said opposing surfaces.

Claim 7 (canceled)

Claim 8 (previously canceled)

Claim 9 (canceled)

Claim 10 (previously amended) The electronic package of Claim 6 wherein respective ones of said copper pads on said one of said surfaces are connected to respective ones of said array of conductive pads on said chip die by a copper plated connection.

Claim 11 (original) The electronic package of Claim 5 wherein said flexible layer is a low elastic modulus material.

Claim 12 (original) The electronic package of Claim 5 wherein said flexible layer has an elastic modulus in the range of 50,000 to 400,000 psi.

Claim 13 (previously amended) The electronic package of Claim 6 wherein said copper plated vias are filled with solder.

Claims 14 - 22 (withdrawn).

REMARKS

Applicants note that Applicants' request of April 9, 2003 for reconsideration of the finality of the March 25, 2003 rejection was considered persuasive by the Examiner and, therefore, the amendments to the claims made in that request have presumably been entered.

By this amendment Claims 2, 7 and 9 have been canceled and Claims 1, 3, 5 and 6 have been amended.

The 35 USC 112 Rejection

The Examiner has rejected Claims 1 - 7 and 9 - 13 under 35 USC 112, first paragraph, as failing to comply with the written description requirement. The Examiner further states, in this regard, that the claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The Examiner goes on to state that the "specification indicated that the sloped vias are provided additional freedom to flex both horizontally and vertically, but there is no support in this specification that the interposer be allowed to flex both vertically and horizontally".

Applicants do not fully understand the Examiner's position in regard to the 35 USC 112 rejection. Applicants' specification calls for an interposer fabricated from a flexible dielectric layer of a low modulus material. Examples of such material are given as

Rogers 2800 material, Dow 1-4173 material and GE 3281 material. Such flexible materials would have a low modulus in any direction since they are isotropic solids, as it were. In order for such compliant material to compress or yield vertically, it must also yield horizontally. The Sado patent relied upon by the Examiner discusses such a characteristic.

Applicants' specification states that the advantage of the sloped plated vias in the compliant interposer is that "this configuration provides additional freedom to flex both vertically and horizontally" (page 7, line 25 et seq.). The vias, plated to the walls of the flexible interposer, cannot flex both vertically and horizontally without the flexible interposer flexing both vertically and horizontally. The flexible interposer must, of necessity, flex both horizontally and vertically if the sloped vias have components of movement in both the X and Y direction.

Accordingly, Applicants believe that it is clear from the described structure that the interposer flexes both vertically and horizontally. This is self-evident and inherent from the description of the structure provided in the specification. To require that the specification state that the interposer is allowed to flex both vertically and horizontally is to state the obvious and would be superfluous.

It should be noted that, consistent with the concept here, is Applicants' description of providing additional holes or vias around the plated vias to form a "swiss cheese like" structure which acts to make the flexible dielectric "more soft and spongy". Clearly, the holes act to provide additional space for the interposer to horizontally expand into upon compliance or compression. Applicants also point out in their specification, that such additional holes may be formed to have the same slope as the plated vias.

The 35 USC 103(a) Rejections

The Examiner has rejected Claims 1, 2, 3, 5, 6 and 10 under 35 USC 103(a) as being unpatentable over Arnio, et al. ('359) in combination with Stone ('416). It is apparently the Examiner's position that Claims 1, 2, 3, 5, 6 and 10 are anticipated by Arnio, et al. except for the claim recitation calling for a "circuit card" whereas Arnio, et al. discloses connection to a "circuit board".

It appears, however, that the Examiner, in this rejection, has overlooked certain specifically recited limitations in these claims. For example, Claims 2 and 6 specify that the copper plated vias terminate "in a copper pad". Arnio, et al. does not teach such an arrangement. Similarly, Claim 10 calls for a copper plated connection, not taught by Arnio, et al. As a further example, Claim 3 has recitation which states that "said dielectric material has an array of holes therethrough positioned between said array of copper plated vias". This is shown in Figure 2 of Applicants' specification. The purpose of such holes is stated on page 7 of Applicants' specification, as discussed above. Arnio, et al. fails to teach or suggest such an arrangement.

The Examiner has also rejected Claims 4, 11 and 12 under 35 USC 103(a) "as being unpatentable over Arnio, et al. as applied to claim 3 or 5 and in further combination with Jimarez, et al." ('952). The Examiner states that Arnio, et al. do not explicitly disclose that the elastomer has a "low modulus in the range of 50,000 to 400,000 psi" but that "Jimarez, et al. utilize silicone with a low modulus of 50,000" and to use such in Arnio, et al. would be obvious.

It should be noted, again, that the limitations of Claim 3, from which Claim 4 depends, recites limitations not found in any reference relied upon by the Examiner. In addition, the dependent claims rejected here call for a modulus in the range of 50,000 to 400,000 while the range taught by Jimarez is 50,000 to 20,000 psi. Thus, the Jimarez, et al. range goes in the direction opposite to the range taught by Applicants. Thus, it is clear that Jimarez, et al. fail to teach or suggest the modulus range taught and claimed by Applicants.

Claim 7 has been rejected under 35 USC 103(a) as being unpatentable over Arnio, et al. and Stone as applied to Claim 5, and in further combination with Sado ('165).

The Examiner is again relying upon Sado for V-shaped metal plated vias. In this regard, the Examiner states that it would be obvious to form V-shaped vias in Arnio, et al. "in order to facilitate absorption of local stress as taught by Sado (Abstract)".

As Applicants pointed out in their January 23, 2003 amendment, the Sado interconnector is designed to overcome the problem of stretching of the rubber matrix due to the pressure required to obtain reliable connection between the two circuit boards. To limit this stretching, Sado employs at least one sheet member having a higher rigidity than the rubber matrix attached thereto. To provide additional rigidity, Sado uses curved linear conductive bodies 2 which make connection between circuit boards. As stated by Sado in col. 3, line 52, et seq. "the configuration of the linear conductive bodies ... is not necessarily straightforward but may be curved or bent". Sado goes on to state that "such a curved or bent configuration is rather preferable since the elastic resilience of the linear bodies can be effectively utilized when the interconnector is mounted between the two

circuit boards" (emphasis added). Sado again refers to such utilization in col. 5, lines 11, et seq.

Thus, it appears that Sado is bending the conductive bodies to add resilience to the rubber matrix which is consistent with Sado's overall objective of adding resilience to that rubber matrix so as to avoid the problems incident stretching. Sado, then, is using what might loosely be called a V-shaped conductor to increase the resilience of the elastic material while Applicants are using this shape to facilitate resilience, i.e., decrease resilience. It should be noted that the linear conductive bodies of Sado are not copper plated vias with its attendant low resilience, as taught by Applicants, but are rather carbon fibers prepared by carbonization or graphitization of organic fibrous materials, etc., or metallic filaments or ribbons. These materials apparently act to provide more resilience than copper plated vias.

The Examiner states that it would be obvious to form the through hole of Arnio, et al. V-shaped "in order to facilitate absorption". Contrary to the Examiner's position, this is apparently not what Sado is doing, i.e., facilitating absorption. Again, Sado rather appears to be increasing the amount of absorption of elastic material, consistent with his objectives of overcoming the stretching problem.

Given what Sado is doing with his so-called "V-shaped" conductors, and given the fact that Arnio, et al. slope their vias to provide good wiping contact and recovery capability, there would be no reason to combine the teachings of Sado in Arnio, et al.

The Examiner has, again, taken a position in regard to the V-shaped vias based upon some notion of criticality. In this regard, the Examiner states that "it would have been an obvious matter of design choice bounded by well known manufacturing

constraints and ascertainable by routine experimentation and optimization to choose the particular dimensions of a sloped via or V-shaped via because Applicants have not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facia that the process would possess utility using another dimension". (Query: what dimension?)

Again, this position is not understood. Insofar as Applicants are aware, "dimensions" go to size not shape of a structure. Applicants are claiming the shape of the via structure when they recite "V-shaped metal plated vias". Applicants are not claiming any dimensions for the vias. Dimensions would seem to go to diameter, length, etc.

The Examiner states that Applicants have "not disclosed that the dimensions are for a particular unobvious purpose". Although defining the shape of the via structure has little to do with reliance on dimensions for patentability or the normal questions of criticality when so relying, there is, however, an important advantage to using the V-shaped via structure. As pointed out on page 8 of Applicants' specification, not only do the V-shaped via configuration allow for additional freedom to flex in both the vertical and horizontal directions but has the additional advantage of positioning pads 19 and 21 in vertical alignment with one another. Thus, the V-shaped vias of Fig. 4 are provided for the same reason the sloped via of Fig. 3 are provided, but also for the additional reason that they allow vertical alignment of contacts between chip and circuit card.

Claim 9 has been rejected under 35 USC 103(a) as being unpatentable over Arnio, et al. in further combination with Brodsky ('691). The Examiner states that it would be obvious to incorporate an array of holes in the interposer of Arnio, et al. in order to reduce stress as taught by Brodsky.

The array of holes of Brodsky are really elongated apertures that surround an offset contact. The contact 56 - 57 of Brodsky is offset from the Brodsky plated through holes 63. Thus, the so-called holes of Brodsky are not "positioned between said array of copper plated vias", as recited in Claim 9. Such can more clearly be seen in Figs. 9 and 10 of Brodsky.

Applicants' arrangement of holes uniformly improves the resilience of the whole interposer and is not localized at the point of electrical contact offset from the interconnecting vias, as shown in Brodsky. Thus, using the teachings of Brodsky in Arnio, et al. would, in fact, not anticipate Applicants' claimed invention.

The Examiner has also rejected Claim 13 under 35 USC 103(a) as unpatentable over Arnio, et al. and Stone as applied to Claim 6 in further combination with Isaacs, et al. ('330). The Examiner is apparently relying on Isaacs for a "PTH filled with solder".

The PTH's of Isaacs, however, are not formed in an flexible interposer but rather are formed in a multi-layer printed circuit board. Moreover, the PTH's are not sloped or V-shaped. The fact that Isaacs happens to fill PTHs with solder has little to do with using solder filled vias in a flexible interposer for connecting a chip to a circuit card.

Applicants' Amended Claims

Although Applicants firmly believe that the amended claims set forth in the April 9, 2003 amendment are allowable as presented, in order to expedite prosecution Applicants have further amended the independent claims to recite patentable limitations of previously presented dependent claims. Thus, Claim 1 has been amended to include the limitations of

canceled Claim 2, and Claim 5 has been amended to include the limitations of canceled Claims 7 and 9. In addition, the recitation of the added limitations has been set forth more particularly than the manner it was set forth in the canceled dependent claims.

Claim 1 now recites "a layer of elastic dielectric material having an array of copper plated vias filled with solder" with "said layer of elastic dielectric material further having a uniform array of holes extending therethrough and arranged so that individual ones of said array of holes are positioned to be substantially surrounded by individual ones of said array of copper plated vias so as to further facilitate uniform compliance of said interposer" (emphasis added).

Claim 3 now recites wherein "said elastic dielectric material having an array of holes extending therethrough positioned to be substantially surrounded by individual ones of said array of copper plated vias are arranged with a slope substantially the same as the slope of said copper plated vias" (emphasis added). Support for this may be found on page 8, lines 1 - 3 of Applicants' specification.

Claim 5 now includes the limitations similar to those set forth in Claim 1 and further including the V-shaped structure of canceled dependent Claim 7, along with chip and circuit card connections.

Since none of the references relied upon by the Examiner teach using an array of holes, arranged as claimed to further facilitate uniform compliance, or V-shaped vias arranged to both facilitate compliance and provide alignment of electrical contacts on opposing surfaces, independent claims 1 and 5, as now presented, are clearly allowable.

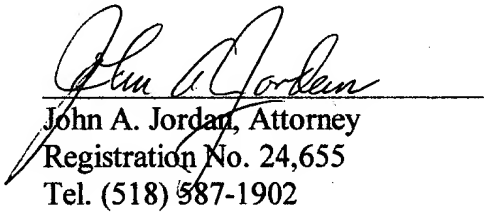
In view of the Examiner's earlier restriction requirement, Applicants retain the right to present Claims 14 - 22 in a divisional application.

In view of Applicants' amendment and remarks, Applicants firmly believe that the application is now in condition for allowance. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the outstanding rejection, allow the claims as presented and pass the case to issue.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

Mark V. Pierson, et al.

By: 

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